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Atty. Dkt No. INFN/SZ0021

IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) A method of operating a double data rate memory device, comprising:

providing a bi-directional line in a system bus of the memory device to transmit a WAIT_DQS signal, the WAIT_DQS signal comprising functionality of (i) a WAIT signal indicating when valid data is present on a data bus in Read cycle and when a memory is ready to accept data in Write cycle, and (ii) a data strobe (DQS) signal serving as a timing signal for valid data; and

propagating the WAIT_DQS signal in a bi-directional line in a system bus of the memory device, wherein the bi-directional line is coupled to the memory and a system controller, and wherein the WAIT_DQS signal has a WAIT state until completion of a refresh operation, in the event that a read cycle collides with an execution of the refresh operation.

2. (Original) The method of claim 1 wherein the memory comprises at least one component memory configured to initiate the WAIT_DQS signal and respond to the received WAIT_DQS signal.

3. (Original) The method of claim 1 wherein:

the at least one component memory further comprises a terminal for transmitting the WAIT_DQS signal to the bi-directional line; and

wherein the bi-directional line is electrically biased to facilitate a logic OR connection between the system controller and the at least one component memory.

4. (Original) The method of claim 1 wherein the memory device operates in a variable latency mode during a read cycle.

5. (Original) The method of claim 1 further comprising:

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initiating the WAIT_DQS signal in the memory.

6. (Original) The method of claim 5 wherein the WAIT_DQS signal further comprises:

- a preamble period;
- a data validation period; and
- a postamble period.

7. (Original) The method of claim 6 wherein, during the preamble period, the WAIT_DQS signal asserts logic low for a duration of one clock cycle on a clock signal that precedes the clock signal when the latency elapses or the memory is ready to output first valid data.

8. (Original) The method of claim 6 wherein, during the data validation period, the WAIT_DQS signal is edge-aligned to data output and toggles between logic low and logic high at every phase of data output to enable the system controller to strobe valid data.

9. (Original) The method of claim 6 wherein, during the postamble period, the WAIT_DQS signal asserts logic low for a duration of one clock cycle following output of last valid data.

10. (Original) The method of claim 1 wherein the memory device is capable of operating in a fixed or variable latency mode during a write cycle.

11. (Original) The method of claim 1 further comprising:
initiating the WAIT_DQS signal in the system controller.

12. (Original) The method of claim 11 wherein the WAIT_DQS signal further comprises:

- a preamble period;

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a data validation period; and
a postamble period.

13. (Original) The method of claim 12 wherein, during the preamble period, the WAIT_DQS signal asserts logic on a clock signal preceding the clock signal when the latency elapses or the memory is ready to ready to first valid data input.

14. (Original) The method of claim 12 wherein, during the data validation period, the WAIT_DQS signal is center-aligned to data input and toggles between logic low and logic high to enable the memory to strobe valid input data.

15. (Currently Amended) A system for controlling memory capable of operating in a double data rate mode comprising:

a memory;
a system controller;
a data bus between the memory and the system controller; and
a system bus between the memory and the system controller, the system bus having a bi-directional line for transmitting a WAIT_DQS signal that combines functionality of a data strobe signal and a wait signal indicating when valid data is present on the data bus during a read cycle and when the memory is ready to accept data during a write cycle, wherein the WAIT_DQS signal has a WAIT state until completion of a refresh operation, in the event that a read cycle collides with an execution of the refresh operation.

16. (Original) The system of claim 15 wherein, at different times, the WAIT_DQS signal is initiated by the memory or the system controller.

17. (Original) The system of claim 15 wherein the WAIT_DQS signal comprises functionality of (i) a WAIT signal indicating when valid data is present on a data bus in Read cycle and when the memory is ready to accept data in Write cycle, and (ii) a data strobe (DQS) signal indicating presence of valid data.

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18. (Original) The system of claim 15 wherein the bi-directional line replaces at least one of a line propagating the DQS signal and a line propagating the WAIT signal.

19. (Original) The system of claim 15 wherein the WAIT_DQS signal is a 3-state digital signal having a logic low active state.

20. (Original) The system of claim 15 wherein the memory comprises at least one component memory configured to initiate the WAIT_DQS signal and respond to the received WAIT_DQS signal.

21. (Currently Amended) A memory device capable of operating in a variable latency mode comprising:

one or more memory cells;

one or more data lines for communicating with a memory controller via a data bus; and

one or more control lines for communicating with the memory controller via a command bus, the one or more control lines comprising a bi-directional line for transmitting a WAIT_DQS signal to the controller and receiving a WAIT_DQS signal from the memory controller, wherein the WAIT_DQS signal combines functionality of a data strobe signal and a wait signal indicating when valid data is present on the data bus during a read cycle and when the memory device is ready to accept data during a write cycle, and wherein the WAIT_DQS signal has a WAIT state until completion of a refresh operation, in the event that a read cycle collides with an execution of the refresh operation.

22. (Original) The memory device of claim 21, wherein the bi-directional line is electrically biased to facilitate a logic OR connection between the system controller and at least one other memory device.

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23. (Original) The memory device of claim 21 wherein the memory device operates in a variable latency mode in Read cycle.

24. (Original) The memory device of claim 23 wherein the WAIT_DQS signal further comprises:

- a preamble period;
- a data validation period; and
- a postamble period.

25. (Original) The memory device of claim 24 wherein, during the preamble period, the memory device asserts the WAIT_DQS signal low for a duration of one clock cycle on a clock signal that precedes the clock signal when the latency elapses or the memory device is ready to output first valid data.

26. (Original) The memory device of claim 24 wherein, during the data validation period, the WAIT_DQS signal is edge-aligned to data output and toggles between logic low and logic high at every phase of data output to enable the memory controller to strobe valid data.

27. (Original) The memory device of claim 24 wherein, during the postamble period, the memory device asserts the WAIT_DQS signal low for a duration of one clock cycle following output of last valid data.

28. (Original) The memory device of claim 21 wherein the memory device operates in a fixed latency mode in Write cycle.

29. (Original) The memory device of claim 28 wherein the WAIT_DQS signal further comprises:

- a preamble period;
- a data validation period; and
- a postamble period.

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30. (Original) The memory device of claim 29 wherein, during the preamble period, the WAIT_DQS signal asserts logic on a clock signal preceding the clock signal when the latency elapses or the memory is ready to ready to first valid data input.

31. (Original) The memory device of claim 29 wherein, during the data validation period, the WAIT_DQS signal is center-aligned to data input and toggles between logic low and logic high to enable the memory to strobe valid input data.

32. (Original) The memory device of claim 29 wherein, during the postamble period, the WAIT_DQS signal asserts logic low for a duration of one clock cycle following input of last valid data.

33. (Original) The memory device of claim 21 wherein the memory device operates in a variable latency mode in Write cycle.

34. (Original) The memory device of claim 33 wherein the WAIT_DQS signal further comprises:

- an indicating period;
- a preamble period;
- a data validation period; and
- a postamble period.

35. (Original) The memory device of claim 34 configured in Write cycle to:
initiate the WAIT_DQS signal during the indicating period; and
receive the WAIT_DQS signal from the system controller during the preamble period, data validation period, and postamble period.

36. (Original) The memory device of claim 34 wherein, during the indicating period, the memory device asserts the WAIT_DQS signal low for a duration of one clock cycle starting two clock cycles prior to beginning of the preamble period.

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37. (Original) The memory device of claim 34 wherein, during the indicating period, the memory device asserts the WAIT_DQS signal low for a duration of one clock cycle starting one clock cycle prior to beginning of the preamble period.

38. (Original) The memory device of claim 34 wherein, during the preamble period, the memory device asserts the WAIT_DQS signal low for a duration of one clock cycle on a clock signal that precedes the clock signal when the latency elapses or the memory device is ready to receive a first valid data input.

39. (Original) The memory device of claim 34 wherein, during the data validation period, the WAIT_DQS signal is center-aligned to data input and toggles between logic low and logic high to enable the memory to strobe valid input data.

40. (Original) The memory device of claim 34 wherein, during the postamble period, the memory device asserts the WAIT_DQS low for a duration of one clock cycle following input of last valid data.